Claim(s)

What is claimed is:

1. A method for measuring resistance of signal paths within an interconnect structure for linking I/O ports of a plurality of channels of an integrated circuit (IC) tester to a plurality of first test points arranged on an IC to be tested, the method comprising the steps of:

a. providing a comparator within each channel for producing a state signal indicating whether a voltage of the channel's I/O port exceeds a reference voltage;

b. providing a driver within each of said channels that can be signaled to selectively provide a digital test signal at the channel's I/O port, to supply a constant current to said I/O port, to connect said I/O port to a reference potential and to tristate said I/O port;

c. providing a plurality of second test points in an arrangement substantially similar to an arrangement of said first test points on said IC; and

d. providing a conductor linking said second test points;

e. employing said interconnect structure to interconnect ones of said second test points with I/O ports of ones of said channels.

2. The method in accordance with claim 1 further comprising the step of:

f. signaling the driver of a first channel of said channels to supply said constant current to the first channel's I/O port.

3. The method in accordance with claim 2 further comprising the step of:

g. signaling the driver of a second channel of said channels to connect the I/O port of said second channel to said reference potential.

4. The method in accordance with claim 3 further comprising the step of:

h. signaling drivers of others of said channels to tristate their I/O ports, such that substantially all of the constant current supplied to said first channel's I/O port passes between said first channel's I/O port and said second channel's I/O port via said interconnect structure and said conductor.

5. The method in accordance with claim 4 further comprising the step of:

i. altering the reference voltage supplied to the comparator of one of said channels and monitoring the state signal produced thereby to determine a port voltage at the I/O port of said one of said channels produced in response to said constant current.

6. The method in accordance with claim 5 further comprising the step of:

j. calculating a signal path resistance in accordance with magnitudes of the port voltage, and said constant current.

7. The method in accordance with claim 4 further comprising the step of:

i. altering the reference voltage supplied to the comparator of a one of said channels and monitoring the state signal produced thereby to determine a first port voltage at the I/O port of said one of said channels produced in response to said constant current.

j. altering the reference voltage supplied to the comparator of another of said channels and monitoring the state signal produced thereby to determine a second port voltage at the I/O port of said one of said channels produced in response to said constant current, and

k. calculating a signal path resistance in accordance with magnitudes of the first port voltage, said reference potential, and said constant current.

8. The method in accordance with claim 5 further comprising the steps of:

j. signaling the driver of a third channel of said channels to connect the I/O port of said third channel to said reference potential;

k. signaling drivers of other channels of said channels to tristate their I/O ports, such that substantially all of the constant current supplied to said first channel's I/O port passes between said first channel's I/O port and said third channel's I/O port via said interconnect structure and said conductor; and

l. altering the reference voltage of the comparator of one of said channels and monitoring the state signal produced thereby to determine a second port voltage at the I/O port of said at least one of said channels produced in response to said constant current.

9. The method in accordance with claim 8 further comprising the steps of:

m. signaling the driver of said second channel of said channels to supply said constant current to the second channel's I/O port;

n. signaling drivers of other channels of said channels to tristate their I/O ports, such that substantially all of the constant current supplied to said second channel's I/O port passes to said third channel's I/O port via said interconnect structure and said conductor; and

o. altering the reference voltage of the comparator of one of said channels and monitoring the state signal produced thereby to determine a fourth port voltage at the I/O port of said at least one of said channels produced in response to said constant current.

10. The method in accordance with claim 9 further comprising the step of:

p. calculating at least one signal path resistance in accordance with magnitudes of the first, second and third

port voltages, said reference potential, and said constant current.

11. The method in accordance with claim 1 wherein said IC to be tested is a die on a wafer and wherein said plurality of second test points provided at step c and said conductor provided at step d are implemented on a reference wafer.

12. The method in accordance with claim 11 wherein said reference wafer is substantially similar in size and shape to said wafer.

13. The method in accordance with claim 1 wherein said reference potential is a ground potential.

14. A channel for an integrated circuit tester, the channel comprising:

an input/output (I/O) port;

a first transistor for turning on and off in response to a first control signal supplied thereto, said first transistor having a first terminal linked to said I/O port, and having a second terminal, said first transistor conductively linking said first and second terminals through low impedance when turned on and isolating said first and second terminals through high impedance when turned off;

a second transistor for turning on and off in response to a second control signal supplied thereto, having a third terminal linked to said I/O port, and having a fourth terminal, said second transistor conductively linking said third and fourth terminals through low impedance when turned on and isolating said third and fourth terminals through high impedance when turned off;

reference signal generation means for selectively supplying one of a first reference voltage and a constant current to said fourth terminal selected in response to a third control signal supplied thereto;

a source of second reference voltage;

comparator means linked to said I/O port for producing an indicating signal indicating whether a voltage at said I/O port exceeds an adjustable reference voltage supplied thereto; and

control means for supplying said first, second and third control signals and said adjustable reference voltage to said first and second transistors, said reference signal generation means and said comparator respectively.

15. The channel in accordance with claim 14 wherein said reference signal generation means comprises:

a first voltage source;

a current source; and

means for alternatively connecting either one of said first voltage source and said current source to said second terminal in response to said third control signal.

16. The channel in accordance with claim 14 wherein said means for applying said second reference voltage to said fourth terminal comprises:

a node at ground potential;

a source of said second reference voltage, and

switch means for selectively linking either of said source of second reference voltage and node to said fourth terminal in response to said third control signal.